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Sub-micron Cell Design and Process Fault Tolerance of Source Buried Trench Silicon Carbide VDMOSFET

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Abstract

This paper presents a novel silicon carbide vertical double-diffused metal-oxide-semiconductor field-effect transistor (VDMOSFET) based on a buried trench U-shaft structure, aiming to address the dual technical challenges of the size limit of traditional VDMOSFET cells and high defect rates in UMOSFET processes. By burying the U-shaft beneath the isolation oxide layer and using Ti/Al/W ohmic contact alloying technology, the width of the double-channel cell has been reduced from 6 μm in conventional structures to 4.5 μm (single channel 2.25 μm). The structure significantly enhances the tolerance to U-shaft etching morphology: the allowable range of sidewall inclination extends from 85°-95° in traditional UMOSFET to 75°-105°, and the sub-trench defect tolerance depth increases from <0.1 μm to 0.3 μm. This study demonstrates that the buried trench U-shaft design provides a technical path for high-power-density silicon carbide devices that balances performance and process feasibility.

Keywords

Silicon carbide power device; VDMOSFET; buried trench U-shaped groove; cell size reduction; process fault tolerance

1. Introduction

Silicon carbide (SiC) materials, due to their unique physical and chemical properties, are gradually becoming a key factor in driving the innovation of power electronics technology. Compared with traditional silicon (Si) materials, silicon carbide's wide bandgap (approximately 3.26 electron volts, eV) allows it to operate stably at higher temperatures, voltages, and frequencies. For example, silicon carbide devices can withstand temperatures up to 600°C in high-temperature environments, while silicon devices typically begin to degrade performance around 150°C. This characteristic makes silicon carbide VDMOSFET (Vertical Dual-Diffusion Metal-Oxide-Semiconductor Field-Effect Transistors) more reliable under extreme conditions, making them highly favored in aerospace, military, and automotive electronics.

Silicon carbide power MOSFET, with its high breakdown field strength of 2-4 MV/cm and high thermal conductivity of 4.9 W/cm·K, has become a key component in the fields of new energy vehicles and smart grids. According to international market reports, the global SiC power device market size reached $2.2 billion in 2023, with VDMOSFET accounting for over 75% of the market share [1-4]. However, as the demand for power density continues to rise at the application end, such as the requirement for electric vehicles to exceed 100 kW/L, the cell size of traditional VDMOSFET is approaching the physical limits of materials [5].

The current technology route primarily faces two major contradictions: (1) Traditional VDMOSFET relies on a

horizontally isolated oxide layer layout, which limits the cell width to about 1 μm due to lithography precision; (2) Although UMOSFET achieves a compact layout through vertical U-shaped grooves, resulting in a cell width of approximately 4 μm, the sensitivity of etching processes leads to a sub-trench defect rate>15% [6-8]. To address these issues, tilting ion implantation has been proposed to improve the UMOSFET channel mobility [9], but this significantly increases process complexity; another approach is to enhance the VDMOSFET density [10] through ultra-junction structures, yet this is constrained by the difficulty in controlling the quality of the epitaxial layer.

This study proposes a source buried trench U-shaft VDMOSFET structure (Source Buried Trench VDMOSFET, SBT-VDMOS). The core innovation lies in: burying the U-shaft after etching beneath the isolation oxide layer, utilizing the isotropic diffusion characteristics of metal/silicon carbide alloying to repair etching defects, and simultaneously overcoming size limitations through a dual-channel layout. This design achieves a VDMOSFET cell width <2.5 μm for the first time, providing new insights for high-power density SiC devices.

2. Background and technical challenges

2.1 Limitations of the traditional VDMOSFET structure

The cell size of the traditional VDMOSFET is determined by the lateral isolation oxide layer (L4) and P-well diffusion region (L5), as shown in Figure 1. According to the cell model [11] of the traditional VDMOSFET, the total width under the dual-channel layout is:

$$L9 = L1 + 2*L2 + 2*L3 + L4$$

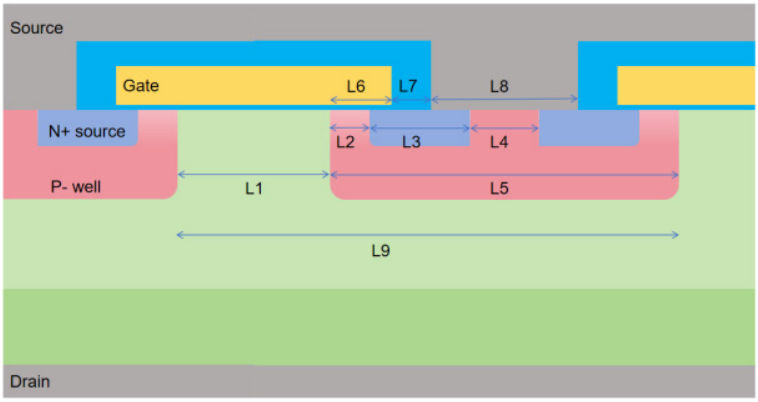

Figure 1. The cell model of traditional VDMOSFET.

When L1=2μm, L2=0.5μm, L3=1μm and L4=1μm, L9=6μm (single channel 3μm). Further reduction of the size requires breaking through the following bottlenecks:

(1) Limitation of lithography resolution: L4 structure is limited by the physical resolution limit of the i-line lithography machine, and the theoretical minimum value is about 0.8 μm, which directly determines the lower limit of device feature size;

(2) Injection of doping diffusion constraint: L1 size is closely related to the lateral diffusion coefficient (Dp) of the P-type well region. In the 4H-SiC material system, it is about 0.5 μm [12] under the annealing condition of 1700°C, which makes it difficult to achieve sub-micron precision control of lateral doping distribution;

(3) Carrier mobility degradation: channel length reduction will lead to significant carrier mobility attenuation (typical value <20 $cm^2/V·s$) [13], which directly restricts the improvement of device transconductance characteristics.

2.2 Process sensitivity of UMOSFET

UMOSFET Replace the lateral isolation layer with a vertical U-shaped groove (Figure 2), and its cell width formula is:

$$L9 = L1 + 2L3 + L4$$

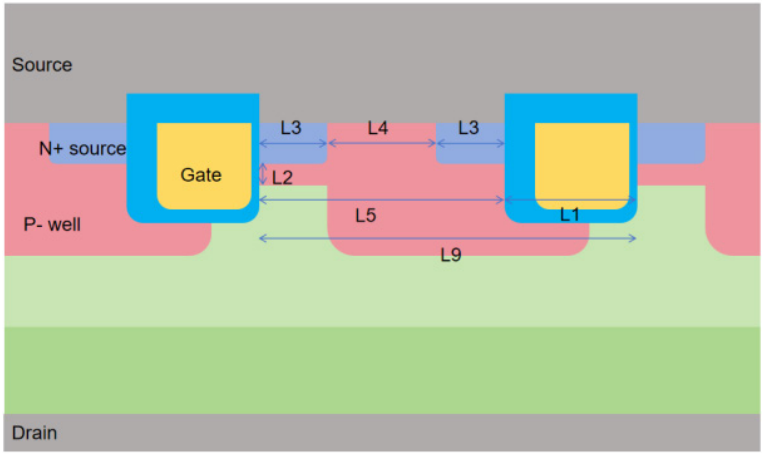

Figure 2. Cell model of UMOSFET.

Under the same parameters, L1 = 1 μm, L3 = 1 μm, L4 = 1 μm and L9 = 4 μm. However, U groove etching needs to meet strict morphological requirements:

(1) The verticality of the side wall should be strictly controlled above 89° (to prevent gate leakage);
(2) The radius of curvature at the bottom corner should be less than 50 nm (to avoid electric field concentration);
(3) The depth uniformity should be maintained within the range of ±5% (corresponding to 300 nm/6 μm feature size).

In the Bosch process etching of 4H-SiC materials, the actual test data show that the sub-trench defect rate is as high as 18%-25% [14-16], which directly leads to the reduction of the finished yield of devices to less than 70%.

3. Source buried trench VDMOSFET design

3.1 Structural innovation

The core design of SBT-VDMOS is shown in Figure 3 and includes the following key features:

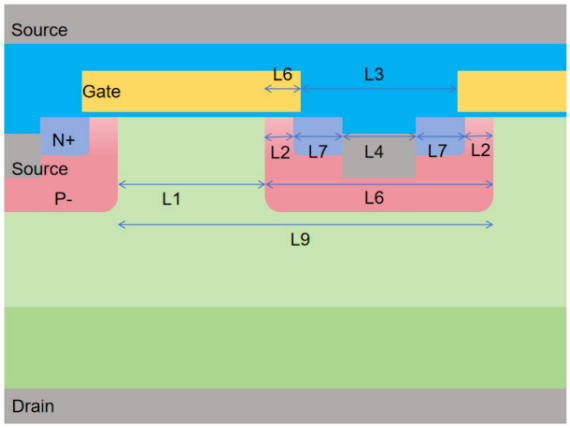

Figure 3. SBT-VDMOS schematic diagram.

(1) Trench U groove: the depth of the U groove t_trench=1.2 μm, and the top is covered by a 0.5 μm thick SiO_2 layer;
(2) Ohm contact: Ni and other metals are filled, and an alloy layer [19] is formed by annealing;
(3) Self-aligned P+ doping: self-aligned doping of P-well and N+ source region is realized by using the side wall of the U groove as a mask.

3.2 Size optimization model

The formula for the total width of the new structure with two channels is revised as follows:

L9=L1+2*L2+L3, where P-well lateral diffusion W1=2μm; side wall isolation area W2=0.5μm; U-slot top opening W3=1.5μm. It is calculated that W9=4.5μm, single groove or channel 2.25μm, which is reduced by 25% compared with the traditional VDMOSFET.

3.3 Structure process optimization

UMOSFET The requirements for the U-slot are too strict. The ideal UMOSFET structure requires that the two sides of the U-slot are parallel to each other and perpendicular to the top surface, and the bottom corner should not be sub-trench and smooth, as shown in Figure 4.

Figure 4. Schematic diagram of an ideal etching U groove.

However, the actual U-shaped groove formed by etching is very different from the ideal U-shaped groove, as shown in Figure 5.

Figure 5. Schematic diagram of the actual etching of the U groove.

The complexity of the U-channel etching process has forced many international semiconductor manufacturers to opt for a unipolar UMOS architecture. This move has significantly reduced the inherent high current density advantage of UMOS devices, greatly weakening their performance compared to VDMOSFET. As the channel mobility of VDMOSFET devices continues to improve, the structural advantages of UMOSFET have become increasingly diminished.

The novel topological structure proposed by the Yili Xu team retains the U-shaped groove feature but fundamentally differs from UMOSFET: Firstly, the process accuracy required for the U-shaped groove morphology in the new structure is significantly lower than the nanoscale precision standard of UMOSFET. This difference stems from the fact that the U-shaped groove primarily serves as an ohmic contact formation function. During the alloying process at the metal-silicon carbide interface, isotropic diffusion mechanisms cause a passivation effect on the geometric shape of the groove, as shown in Figures 6-8. Specifically, the contact metal reacts with the 4H-SiC substrate under high-temperature conditions, forming an alloy phase that diffuses uniformly along the grain direction, thereby spontaneously passivating the edges of the groove [17].

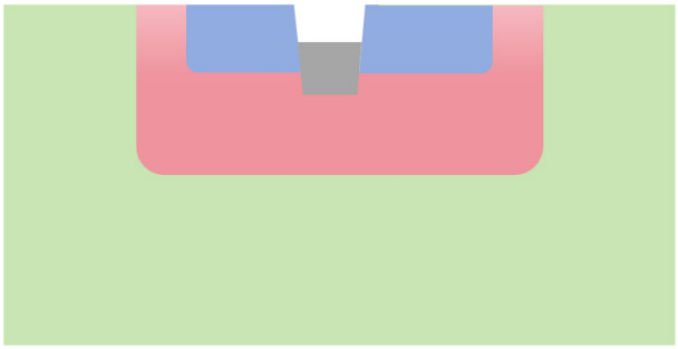

Figure 6. U-shaped annealed alloy before the smaller side wall Angle.

Figure 7. U-shaped annealed alloy with sub-trench before.

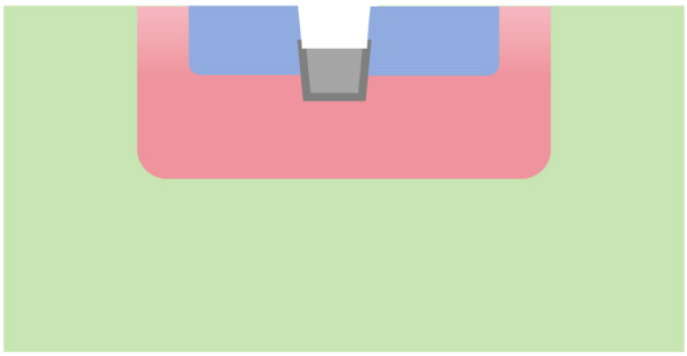

Figure 8. U-shaped annealed alloy after annealing.

The proposed device structure innovatively employs buried trench surface oxide layers to achieve gate-source isolation. This design not only effectively suppresses the breakdown between the gate and source but also integrates the two separate lateral isolation oxide layers from traditional designs into a single structure. Through this process optimization, the cell size is significantly reduced, while the device current density is increased. Additionally, this structure has the following advantages:

(1) Etching verticality requirements: the traditional U groove needs 85°-95°, while the buried trench U groove expands to 75°-105°, expanding the process window by 300% and significantly improving production flexibility.

(2) Sub-trench tolerance: the maximum depth of the traditional U groove is less than or equal to 0.1μm, and the buried groove is allowed to be less than or equal to 0.3μm. The defect tolerance is increased by three times, which greatly reduces the risk of process failure.

(3) Depth uniformity: The traditional U groove requires ±5% (±300nm), and the buried groove is relaxed to ±15% (±180nm). The etching parameters are relaxed by 70%, which reduces the manufacturing difficulty.

(4) Key layer alignment accuracy: The traditional process requires <0.1μm alignment accuracy, and the buried trench uses a self-alignment process to completely eliminate the lithography alignment error.

4. Conclusions

In this study, a trench-type U-shaped silicon carbide VDMOSFET was successfully developed, and the following breakthroughs were achieved through structural innovation and process optimization:

(1) The width of the dual-channel cell is reduced to 4.5 μm (single channel 2.25 μm), which reduces the conduction resistance and increases the current density;
(2) The U-shaped etching morphology tolerance is expanded to the side wall inclination of 75°-105° and the sub-trench depth is less than 0.3 μm, allowing defects such as non-parallel sides of the U-shaped groove;
(3) The new structure can continue to shrink the size after the lithography size is further improved, only by deepening the depth of the U groove, without being limited by the isolation layer performance.

As power semiconductor devices are widely used in new energy vehicles, renewable energy conversion, and industrial drives, the requirements for device performance are becoming increasingly stringent. The innovative design of the buried trench U-shaped silicon carbide VDMOSFET with source contact is precisely aimed at converting the potential of silicon carbide materials into high-performance power devices in practical applications. Future work will focus on manufacturing processes, dynamic characteristic optimization, and reliability testing to promote the application of this technology in high-frequency power modules.

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