Journal of Applied Mathematics and Computation (JAMC), 2018, 2(6), 233-244
http://www.hillpublisher.org/journal/jamc
ISSN Online:2576-0645
ISSN Print:2576-0653

Quadding against Tripling & Deep Tripling

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How to cite this paper: Tyurin, S.F. (2018) **Quadding against Tripling & Deep Tripling**. *Journal of Applied Mathematics and Computation*, **2(6)**, 233-244.
http://dx.doi.org/10.26855/ jamc.2018.06.001
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Abstract

Redundancy is one of the main ways to ensure the reliability of critical equipment, as well as Radiation Hardened by Design, RHBD. They use the Tripling of digital equipment (majoritation), that is, they use, for example, three channels of equipment with a choice of "two out of three" using the so-called Majority Vote Circuit for each bit. In this case, the more Majority Vote Circuits, the greater the gain in the probability of failure-free operation. When the entire device (for example, a computer) is tripled, we obtain a general majoritation. In the case of tripling individual device blocks (for example, processor, memory, I/O, etc.), we obtain a separate tripling. Further deepening of the Tripling leads to the so-called Deep Tripling. In principle, it is possible to triple individual elements. It turns out that the so-called Quadding at an even lower level-CMOS transistor significantly exceeds the element tripling, and sometimes it has even less complexity. The article deals with the features of Tripling and Quadding, the corresponding expressions and graphs are analyzed.

Keywords

Redundancy, Reliability Block Diagrams, Tripling, Deep Tripling, Quadding.

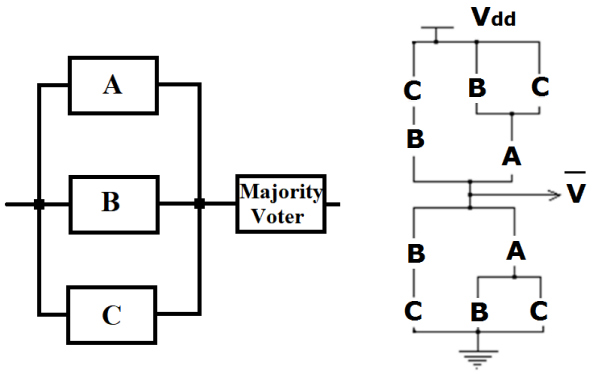
1. Introduction

Reliability is one of the most important indicators of the systems quality, including technical ones. The traditional method of ensuring reliability is the use of structural, temporal or information redundancy. Redundancy is one of the main condition to design a Fault-Tolerant Systems (FTS) [1,2]. For example, Radiation Hardened by Design (RHBD) Systems are Fault-Tolerant Systems [3]. FTS use «Passive Fault Masking (PFM) of the redundant circuits, e.g., by quadding (Quadding Redundancy, QR) or by majority decision circuits, etc. (Patent Class 714/E11.069) » [4]. FTS includes Triple Modular Redundancy (TMR) for the PFM. At the same time Active Fault-Tolerant Systems (AFTS) use «active fault masking, e.g., by switching out faulty elements or by switching in spare elements, etc. (Patent Class 714/E11 » [4]. These systems require considerable time to search for failures and reconfigurations. So consider the fastest PFM Systems. However, TMR – has more than 300% redundancy, QR – has more than 400% redundancy. Greater reliability requires more redundancy, but it is advisable to investigate in detail how much. Perhaps there are special cases when this principle is not fulfilled. Let us investigate and will compare TMR & QR features of the PFM Systems at different levels [5].

2. Method details

Tripling

Tripling (TMR for the A, B, C channels) [5] Conditional Reliability Block Diagram and Decision Circuit shows Fig.1 a), b)



a) b)

Figure 1. Tripling: a) Conditional Reliability Block Diagram; b) CMOS Mirror Majority Vote Circuit (Decision Circuit)

Let us perform arithmetization of the corresponding operability logical function (without Majority Voter) - Fig.1 a):

$$F(ABC) = A \vee B \vee C = (A + B - AB) \vee C =$$
$$= (A + B - AB) + C - (A + B - AB)C =$$
$$= (A + B - AB + C - AC - BC + ABC) \,\&\, (A = B = C) \Rightarrow$$
$$3A - 3A^2 + A^3 = 1 - 1 + 3A - 3A^2 + A^3 =$$
$$= 1 - (1 - 3A + 3A^2 - A^3) =$$
$$= 1 - (1 - A)^3. \tag{1}$$

Passing to probabilities (A=P), we get expression

$$1 - (1 - P)^3. \tag{2}$$

So Fig.1a) is "1 from 3" RBD or ≥ 1 or Active Fault-Tolerant Systems (AFTS):

It is easy to see that real Tripling ≥ 2 Reliability Block Diagrams (Passive Fault Masking, PFM) shows Fig.2

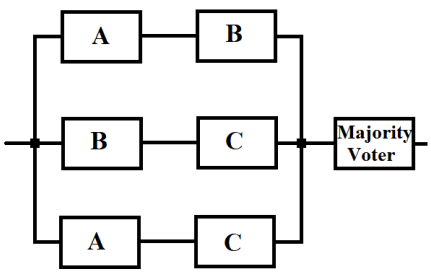


Figure 2. Detail Tripling ≥ 2 Reliability Block Diagrams for A, B, C channels with one Majority Voter (Fig.1b)

The corresponding Fig. 2 real logical function (without Majority Voter) is:

$$AB \vee AC \vee BC = (AB + AC - ABAC) + BC - (AB + AC - ABAC)BC =$$
$$= (AB + AC - ABC) + BC - (AB + AC - ABC)BC =$$
$$= AB + AC - ABC + BC - ABBC + ACBC - ABCBC =$$
$$= AB + AC - ABC + BC - ABC - ABC + ABC =$$
$$= (AB + AC - ABC + BC - ABC - ABC + ABC) \,\&\, (A = B = C) \Rightarrow$$
$$= 3AA - 2AAA = 3A^2 - 2A^3. \tag{3}$$

Passing to probabilities (A=P), we get

$$P_3 = 3P^2 - 2P^3. \tag{4}$$

For example if $P = 0,9$ we have

$$P_3 = 3(0,9)^2 - 2(0,9)^3 = 0,972. \tag{5}$$

So for the different single faults, for example, A channel we get

$$AB \vee AC \vee BC \Rightarrow (1B \vee 1C \vee BC) \& (A = B = C) \Rightarrow$$
$$(1A \vee 1A \vee AA) \Rightarrow A;$$
$$(0B \vee 0C \vee BC) \& (A = B = C) \Rightarrow$$
$$(0A \vee 0A \vee AA) \Rightarrow A;$$
$$(\overline{A}B \vee \overline{A}C \vee BC) \& (A = B = C) \Rightarrow$$
$$(\overline{A}A \vee \overline{A}A \vee AA) \Rightarrow A;$$
$$(XB \vee XC \vee BC) \& (A = B = C) \Rightarrow$$
$$(XA \vee XA \vee AA) \Rightarrow A. \tag{6}$$

In case two, for example, "stuck at 1" faults A=B=1 we have error

$$AB \vee AC \vee BC \Rightarrow (11 \vee 1C \vee 1C) = 1. \tag{7}$$

CMOS Mirror Majority Vote Circuit or Decision Circuit (Fig.1b) implements the dual expression

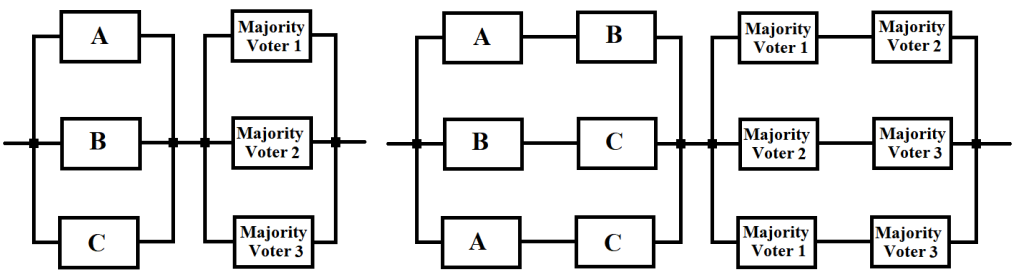
$$\overline{AB \vee AC \vee BC} = \overline{AB}\,\overline{AC}\,\overline{BC} = (\overline{A} \vee \overline{B})(\overline{A} \vee \overline{C})(\overline{B} \vee \overline{C}) =$$
$$= \overline{A}\overline{B} \vee \overline{A}\overline{C} \vee \overline{B}\overline{C}. \tag{8}$$

Taking into account Weibull distribution [6] and Majority Voter's probability we get:

$$P_{*3} = (3 \cdot e^{-2 \cdot (n) \cdot \lambda \cdot t^{\alpha}} - 2 \cdot e^{-3 \cdot (n) \cdot \lambda \cdot t^{\alpha}}) e^{-(12) \cdot \lambda \cdot t^{\alpha}}, \tag{9}$$

λ - is the failure rate of one transistor (dimension 1 / hour), t – is the time, $1 < \alpha < 2$ - is the Weibull distribution coefficient, n –is the number of the transistors in channel.

Mirror Majority Voter has 12 transistors (Fig.1b). Advanced TMR RBD has three Majority Voters-Fig.3:



a) b)

Figure 3. Tripling ≥ 2 Reliability Block Diagrams for A, B, C channels with three Majority Voter a) conditional RBD; b) detail RBD.

With detail ≥ 2 RBD we have

$$P_{*33} = (3 \cdot e^{-2 \cdot (n) \cdot \lambda \cdot t^{\alpha}} - 2 \cdot e^{-3 \cdot (n) \cdot \lambda \cdot t^{\alpha}})(3 \cdot e^{-2 \cdot (12) \cdot \lambda \cdot t^{\alpha}} - 2 \cdot e^{-3 \cdot (12) \cdot \lambda \cdot t^{\alpha}}). \tag{10}$$

In addition, TMR requires three power supplies. Thus, TMR parries either the failure of one power source or the failure of one channel or the refusal of one Majority Voter. The cost C of the tripling system a lot more alone channel:

$$C_{dt} > 3(C_{channel} + C_{\substack{\text{wajority}\\\text{voter}}} + C_{\substack{\text{power}\\\text{supplay}}}). \tag{11}$$

Next redundancy level is "Fiveing" (3 from 5)≥ 3, for example

$$P_5 = P^5 + 5P^4(1-P) + 10P^3(1-P)^2 = (0,9)^5 + 5(0,9)^4(0,1) + 10(0,9)^3(0,1)^2 = 0,99144. \tag{12}$$

Conditional Reliability Block Diagrams ≥ 3 shows Fig.4.

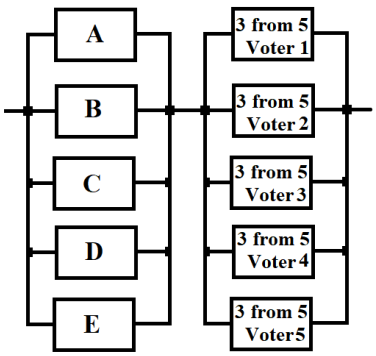


Figure 4. "Fiveing" (3 from 5) ≥ 3 Conditional Reliability Block Diagrams

With detail ≥ 3 RBD and Majority Voter "3/5" we get

$$P_5(t) = e^{-5\lambda t^\alpha} + 5e^{-4\lambda t^\alpha}(1-e^{-\lambda t^\alpha}) + 10e^{-3\lambda t^\alpha}(1-e^{-\lambda t^\alpha})^2 \cdot$$
$$\cdot[e^{-5\lambda_{v3/5} t^\alpha} + 5e^{-4\lambda_{v3/5} t^\alpha}(1-e^{-\lambda_{v3/5} t^\alpha}) + 10^{-3\lambda_{v3/5} t^\alpha}(1-e^{-\lambda_{v3/5} t^\alpha})^2]. \tag{13}$$

In addition, five power supplies are needed. Next Tripling ≥ 1 "At least one channel" (2) most of all increases reliability:

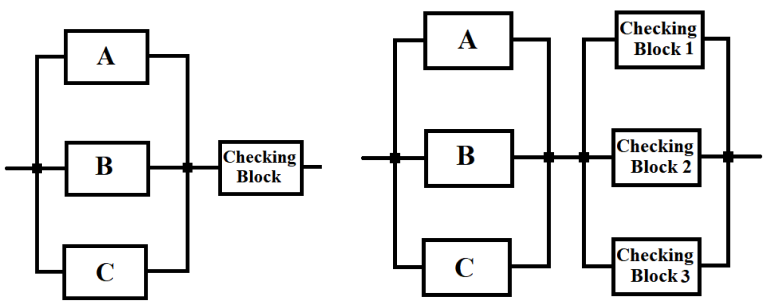
$$P_{\geq 1} = 1-(0,1)^3 = 0,999. \tag{14}$$

However, Tripling ≥ 1 requires special checking block and reconfiguration hardware (cb) shows Fig.5a):

$$P_{\geq 1} = [1-(1-e^{-\lambda t^\alpha})^3]e^{-\lambda_{cb})t^\alpha} \tag{15}$$

Therefore option "At least one channel, at least one checking block"- Fig.5b) and expression

$$P_{\geq 1^*} = [1-(1-e^{-\lambda t^\alpha})^3][1-(1-e^{-\lambda_{cb} t^\alpha})^3]. \tag{16}$$



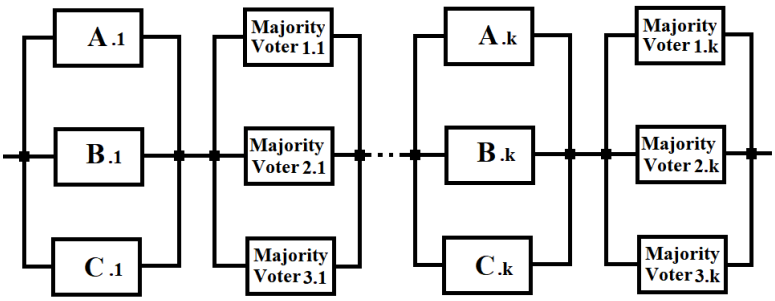
a) b)

Figure 5. Tripling ≥ 1 Detail Reliability Block Diagrams for A, B, C channels: a) RBD with one checking block; b) RBD with three checking block

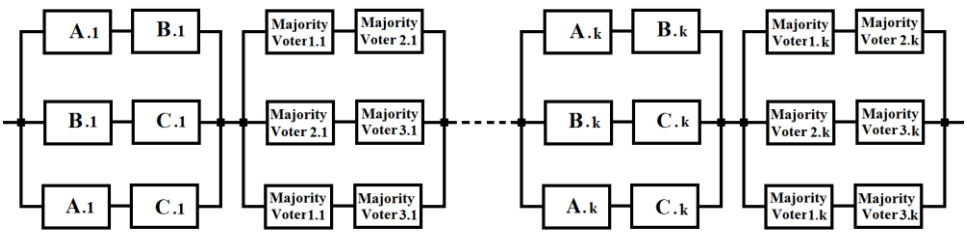
Expression (16) does not take into account the probability of a "miss" in the event that operational testing does not lead to the detection of a failed channel.

Deep Tripling

High Level is Deep Tripling (k-layer Tripling)-Fig.6:



a)



b)

Figure 6. Deep Tripling: a) Conditional Reliability Block Diagrams; b) detail Reliability Block Diagrams

Assume the assumption that λ - the failure rate of the entire channel is divided into k equal parts, then we get λ_{tr}

$$P_{dt} = [3e^{-2n\frac{\lambda}{k}t^{\alpha}} - 2e^{-3n\frac{\lambda}{k}t^{\alpha}}]^k [3e^{-2\cdot 12\lambda_{tr}t^{\alpha}} - 2e^{-3\cdot 12\lambda_{tr}t^{\alpha}}]^k, \tag{17}$$

λ_{tr} - the failure rate of the one of the 12 Majority Voter transistors.

The cost C of the system is increased:

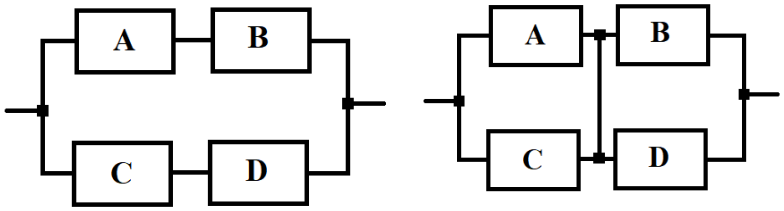
$$C_{dt} > 3(C_{channel} + C_{\substack{\text{power}\\ \text{supplay}}}) + kC_{\substack{\text{wajority}\\ \text{voter}}}, \tag{18}$$

Limit depth - one element, transistors cannot be tripled. In common case "(2r+1)-ing", r-faults number we get:

$$P_{(r+1)\,from\,(2r+1)}(t) = \sum_{i=0}^{r} C_{2r+1}^{i+1} \{e^{-[(2r+1)-i]\cdot\lambda\cdot t^{\alpha}} \cdot (1-e^{-\lambda\cdot t^{\alpha}})^i\}. \tag{19}$$

Quadding

Let A, B, C, D CMOS transistors or CMOS circuits (functions), then quadding [7-10] (r=1) illustrated Fig.7.



a) b)

Figure 7. Quadding: a) DNF option; b) CNF option

Fig.7 is real circuit, not RBD, decision circuit is absent this is done by flowing current in the corresponding CMOS circuit. In disjunctive normal form (DNF) we get expression

$$AB \vee CD, (A = B = C = D) \Rightarrow AA \vee AA = A. \tag{20}$$

With single defect, we have no errors:

$$\begin{gathered} AA \vee A1 = A; AA \vee A0 = A; \\ AA \vee A\overline{A} = A; AA \vee AX = A. \end{gathered} \tag{21}$$

With two defects, for example, we get error:

$$AA \vee 11 = 1. \tag{22}$$

In conjunctive normal form (CNF) we get expression

$$(A \vee B)(C \vee D), (A = B = C = D) \Rightarrow (A \vee A)(A \vee A) = A. \tag{23}$$

Similarly:

$$\begin{gathered} (A \vee A)(A \vee 1) = A; (A \vee A)(A \vee 0) = A; \\ (A \vee A)(A \vee \overline{A}) = A; (A \vee A)(A \vee X) = A; \\ (1 \vee A)(A \vee 1) = 1. \end{gathered} \tag{24}$$

Detail Quadding Reliability Block Diagrams shows Fig.8

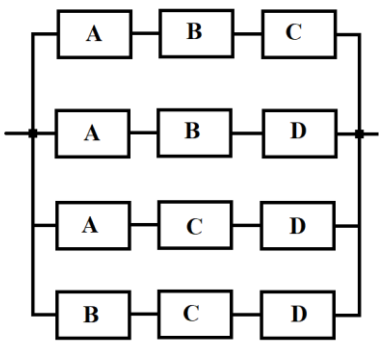
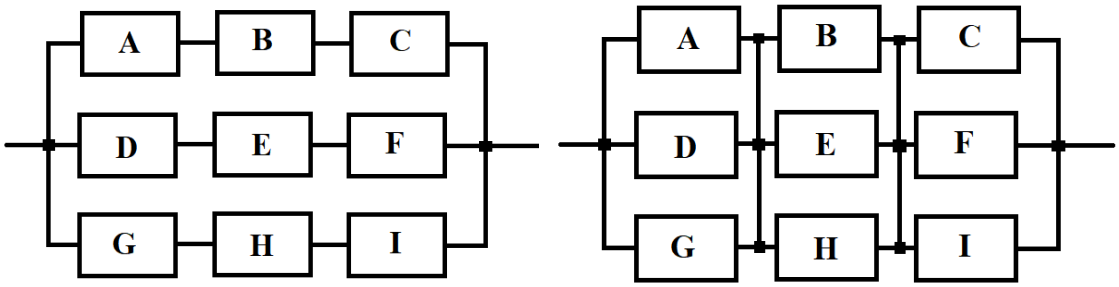


Figure 8. Detail Quadding Reliability Block Diagrams for r=1(A, B, C, D – CMOS transistors or CMOS circuits)

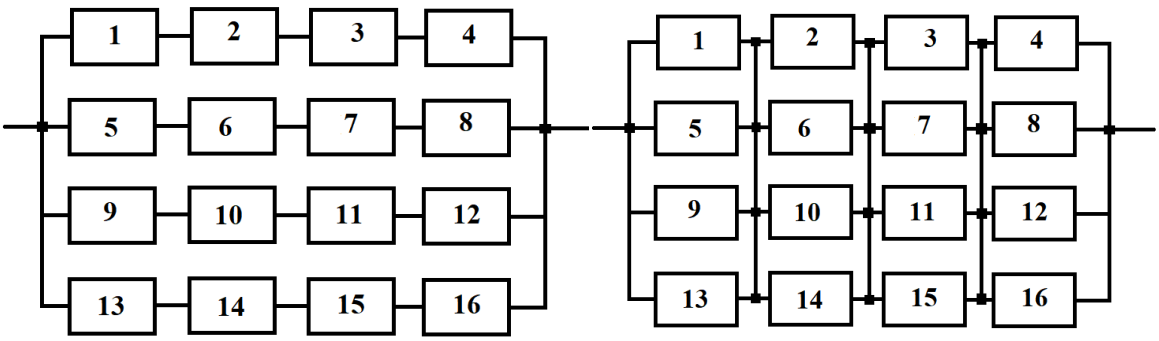
Quadding Circuit for r=2 shows Fig.9



a) b)

Figure 9. Quadding for r=2 (A,B,C,D,E,F,G,H,I – CMOS transistors): a) Quadding Circuit 1; b) Quadding Circuit 2

Quadding Circuit for r=3 shows Fig.10



a) b)

Figure 10. Quadding for r=3 (1,2,3…16 – CMOS transistors): a) Quadding Circuit 1; b) Quadding Circuit 2

Failure-free operation probability of CMOS quadding (r=1) for n transistor has expression:

$$P(t)_{4.tr} = [e^{-4\cdot\lambda\cdot t^{\alpha}} + 4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{n}, \tag{25}$$

And for $n\lambda$ CMOS circuits

$$P(t)_{4.c} = [e^{-4\cdot n\lambda\cdot t^{\alpha}} + 4\cdot e^{-3\cdot n\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]. \tag{26}$$

However, expressions (25), (26) is valid only up to the Mead-Conway constraint $(r+1)n \le q$ restrictions on the maximum number of series-connected transistors $(r+1)n$ in the circuit; they cannot be greater than q [11]. Then for r = 1 we get two original CMOS (n=2) for q=4. For r = 2,3 we get only one original CMOS (n=1) for q=4. This allows you to get no more than only a redundant inverter. However, it is possible to design a LUT for one variable [12-14]. Unfortunately redundancy for r = 4 and more is practically not realizable with modern technologies. Let m - number of circuit outputs (when observing the restrictions of Mead-Conway). CMOS Quadding "not more expensive" than CMOS tripling in case

$$4n \le 3n + 12m \Rightarrow 1 \le 12\frac{m}{n} \tag{27}$$

Failure-free operation probability of channel quadding requires specific CMOS voter circuit [9,10], so

$$P(t)_{4} = [e^{-4\cdot n\lambda\cdot t^{\alpha}} + 4\cdot e^{-3\cdot n\lambda\cdot t^{\alpha}}(1-e^{-n\lambda\cdot t^{\alpha}})]^{n}[e^{-4\cdot\lambda\cdot t^{\alpha}} + 4\cdot e^{-3\cdot\lambda\cdot t^{\alpha}}(1-e^{-\lambda\cdot t^{\alpha}})]^{m}. \tag{28}$$

The quadding circuit delay increases more than 2 times compared to the original circuit. In this way for r>1 we get "$(r+1)^2$-ing" and common expression

$$P_{(r)\,from(r+1)^2}(t)=\sum_{i=0}^{r}C^{i}_{(r+1)^2}\{e^{-[(r+1)^2-i]\cdot\lambda\cdot t^{\alpha}}\cdot(1-e^{-\lambda\cdot t^{\alpha}})^{i}\}. \tag{29}$$

Comparison of the quadding and tripling

Let us get the graphs in the computer mathematics system MathCad. We investigate tripling –Fig.11,12.

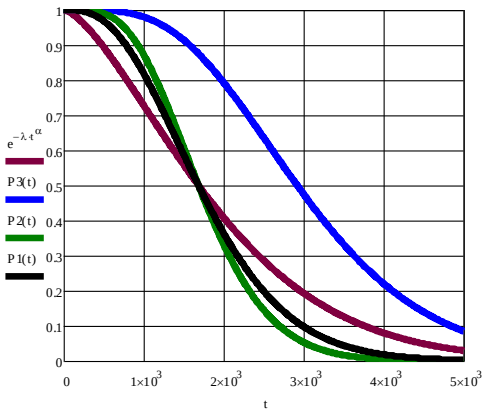
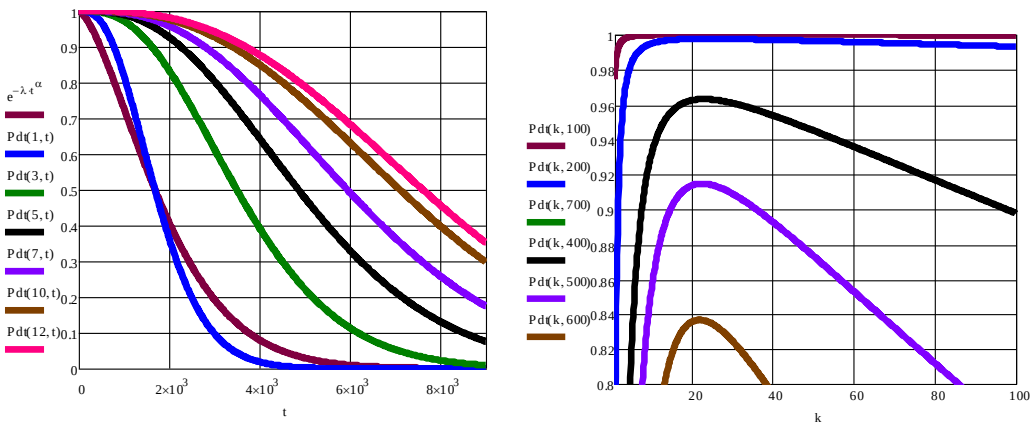


Figure 11. Failure-free operation probability of a original CMOS circuit $e^{-\lambda\cdot t^{\alpha}}$, tripling ≥ 2 $P1(t)$ (black), fiveing $P2(t)$ (green) and tripling ≥ 1 $P3(t)$ (blue), $\alpha = 1,5$.

We see that majority's methods $P1(t)$, $P2(t)$ "raises" the exponent upward beyond a point corresponding to about a third of the time axis (Fig.12 b), but this leads to "sagging" in the last third. Nevertheless, tripling better forever! Deep tripling significantly improves reliability as the k layers increase-Fig 12.



a) b)

Figure 12. Failure-free operation probability of a original CMOS circuit $e^{-\lambda\cdot t^{\alpha}}$ and deep tripling Pdt (k,t); a) k=1,3….12, $\lambda = 10^{-5}; \lambda_{mv} = 10^{-8}; \alpha = 2.$ b) Optimum depends t,k

Note, that Pdt(1,t) is usual tripling (Fig.12). Quadding P4 better than deep tripling P3dt – Fig.13.

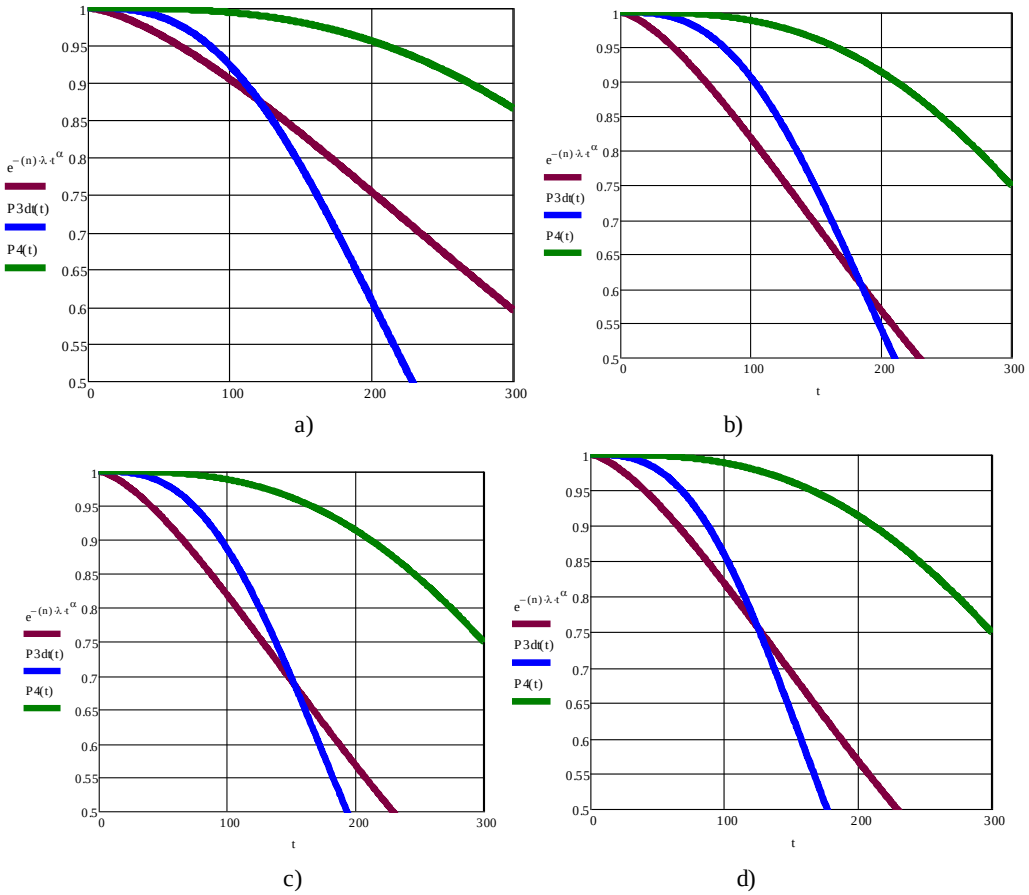


Figure 13. Failure-free operation probability of a original CMOS circuit $e^{-(n)\lambda \cdot t^{\alpha}}$, quadding $P(t)_4$ and deep tripling P3dt: a) n=10, k=2; b) n=20, k=2; c) n=20, k=3; d) n=20, k=4.

A simple tripling P3 is even better than a deep one for small n, but at large n, vice versa-Fig.14.

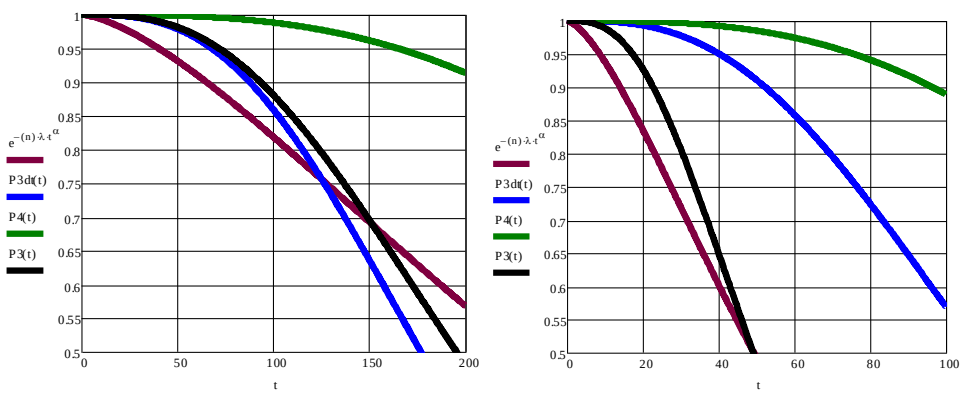


Figure 14. Failure-free operation probability of a original CMOS circuit $e^{-(n)\lambda \cdot t^{\alpha}}$, quadding $P4(t)$ and deep tripling P3dt; a) n=20; b) n=200

Quadding transistors P4tr better than quadding circuits P4c – Fig.15.

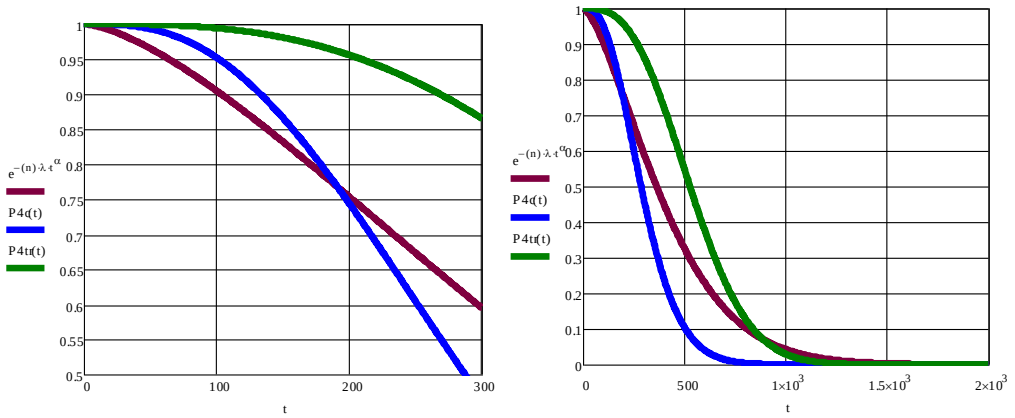


Figure 15. Quadding single transistors P4tr is better quadding circuits P4c, $e^{-n\lambda \cdot t^{\alpha}}$ - original CMOS, n=10

Comparison of the quadding circuits $P4(t)$ with tripling $P3(t)$ (one Majority Voter), $P33(t)$ (three Majority Voter) presents Fig.16.

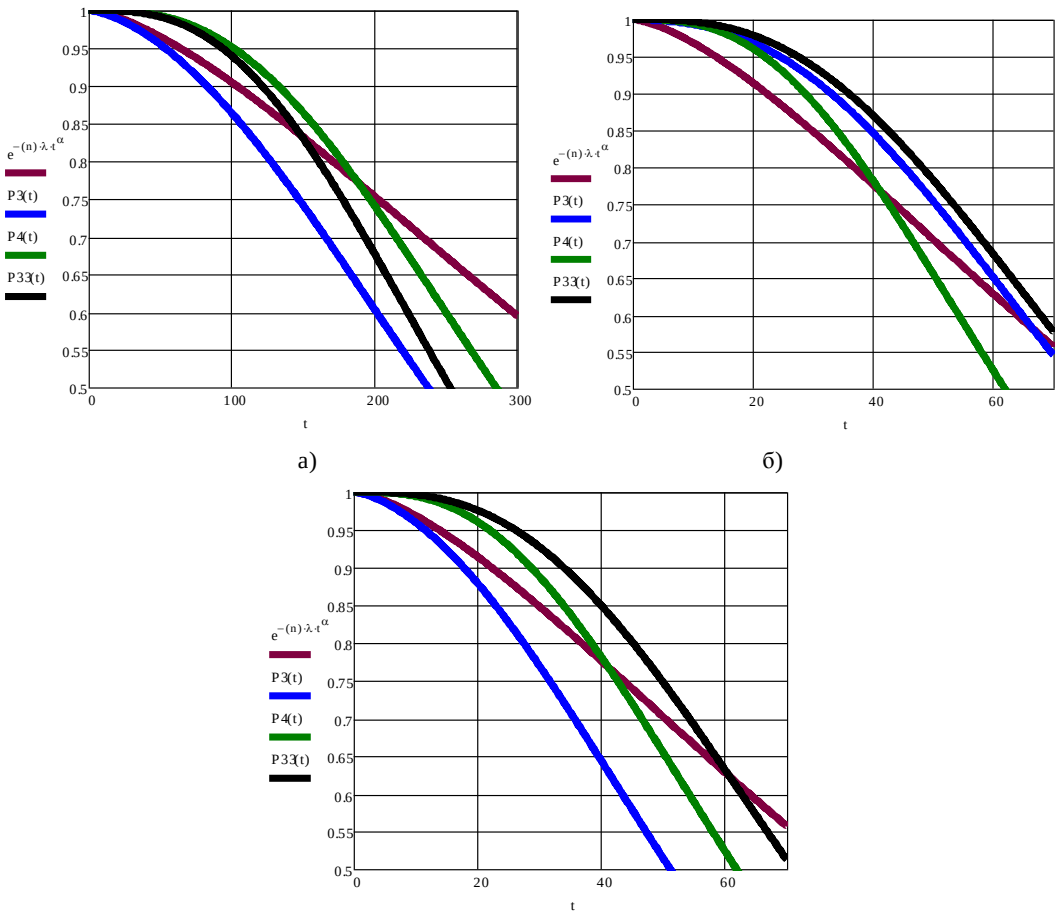


Figure 16. Failure-free operation probability of the quadding circuits: a) n=10, m=1; b) n=100, m=1; c) n=100, m=10; m-number of the circuit outputs.

Conclusion

To increase the reliability at the level of the elements, the most profitable is the deep tripling. For the design of the RHBD equipment, redundancy at the transistor level (quadding) is most effective. Channel quadded-structure cool loses to quadded-transistor and tripling. However, in connection with the limitations of Mead-Conway, it is advisable to combine transistor quadding and deep tripling. In order to parry the failures of the power supply unit, it is possible to use its duplication. Reliability, like money, is never enough. However, optimal solutions are somewhere in the middle and require a combination of redundancy.

In the future, it is necessary to investigate the diagnosis of the quadded-transistor CMOS circuit, for example, using an alternate power supply to the substrates. Particular attention should be paid to the issues of the quadding and deep tripling FPGAs, for example LUT, SRAM, tri-stable buffers.

Acknowledgements

This research was carried out with the support of the Automation and Remote Control Department (Perm National Research Polytechnic University), and the support of the Software Computing Systems Department (Perm State National Research University).

Special thanks to the honored inventor of Ukraine, Doctor of Technical Sciences, Professor Kharchenko Vyacheslav Sergeyevich (National Aerospace University "Kharkiv Aviation Institute"), and to the Doctor of Technical Sciences and Professor Drozd Alexander Valentinovich (Odessa National Polytechnic University) and many others.

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